

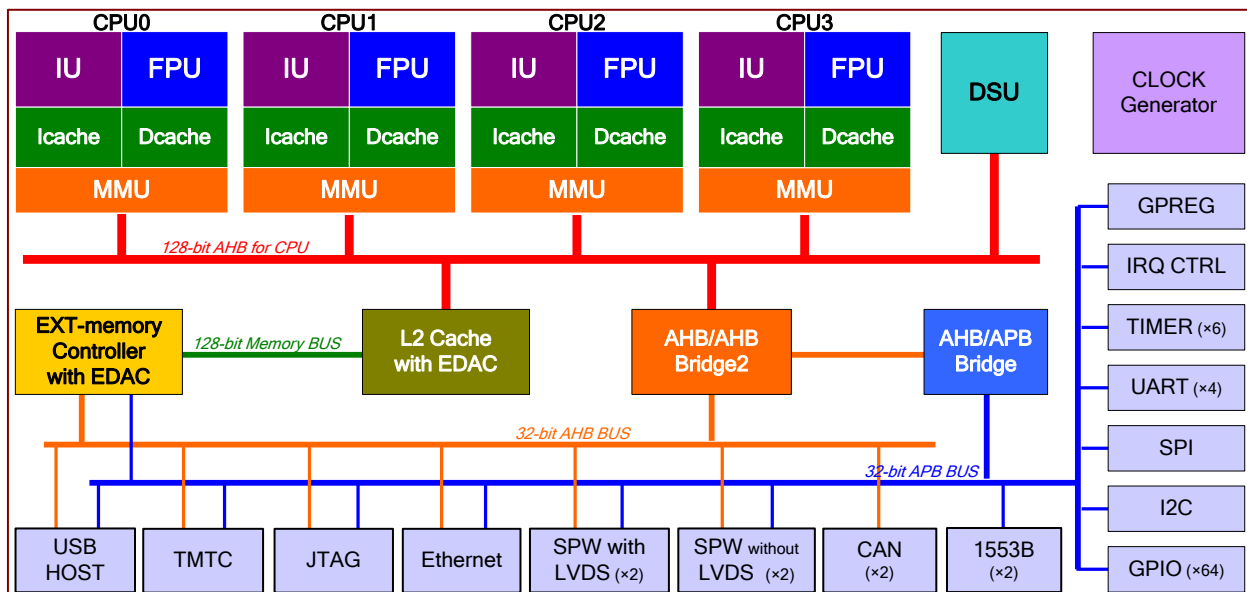
PRODUCT DESCRIPTION

The E698PM Radiation hardened processor is a high performance, high reliability, high integration and low power multi-core SoC. Its symmetric multi-processing (SMP) architecture is compliant with the SPARC V8 standard. It is designed for high-end embedded real-time control and complex computing applications in rugged environments.

The E698PM processor integrates four identical cores, each with an integer unit (IU), a floating point unit (FPU), an level-1 instruction and data cache (ICache & DCache) and a memory management unit (MMU).

The E698PM uses a 128-bit AHB bus for interconnection of its four identical cores, a 32-bit AHB bus for interconnection of its on-chip high-speed peripherals, and a 32-bit APB bus for interconnection of on-chip low-speed peripherals. The E698PM provides many on-chip peripherals, including GPIO, UART, timer, interrupt controller, debug support unit, external memory controller, 1553B BC/RT/BM controller, CAN 2.0 bus controller, 10M/100M Ethernet controller, SpaceWire codec controller, CCSDS TMTc interface, USB 2.0 host controller, SPI master controller and I2C master controller. With the on-chip Debug Support Unit (DSU), the user can access the on-chip registers, memories and peripherals over a UART or Ethernet interface. This provides an excellent software and hardware debugging and development environment.

The E698PM is designed to support eCOS, VxWorks, Linux and other embedded operating systems.



Development Kit

The E698PM development kit contains all the developer needs to get started:-

- E698PM Development Board
- Orion 6 IDE
- DMON Debug Monitor (1 year license)
- Sample C Code
- E698PM Technical Documentation



E698PM

Radiation-hardened SPARC V8 Quadcore Processor SoC

SPECIFICATIONS

Four identical high-performance processor cores each consisting of:	Radiation hardened design
32-bit SPARC V8 integer unit (IU), compliant with IEEE-1754 standard	On-chip flip-flops: TMR
64-bit double precision floating point unit (FPU), compliant with IEEE-754 standard	On-chip memory blocks: EDAC
L1 cache, including instruction cache(ICache) and data cache(Dcache)	External memory Interface: EDAC
Memory Management Unit (MMU)	3-δclock tree
Hardware multiplier and divider	Performance
Supports MAC and UMAC DSP instructions	Max clock speed: 600MHz
7-stage instruction pipeline	2100 MIPS @ 600MHz
On-chip interconnect based on AMBA2 .0	900 MFLOPS@ 600MHz
128-bit AHB for the interconnect of 4 identical processor cores	Power usage
32-bit AHB for the interconnect of high-speed peripherals	2.8W @ 600MHz
32-bit APB for the interconnect of low-speed peripherals	Resilience
AHB I AHB bridge for the data exchange between 128-bit AHB and 32-bit AHB	TID ≥ 300KRad (Si)
AHB I APB bridge for the data exchange between 32-bit AHB and 32-bit APB	SEL ≥ 98Mev-cm ² /mg
Two Level cache structure	SEU ≥ 37Mev-cm ² /mg
L1 Cache: 32KB ICache and 16KB DCache, located in the processor core	Process
L2 Cache: 512KB, located between the memory controller and 12B-bit AHB	Global Foundries 65nm RFCMOS LPe
On-chip peripherals	Operating voltage
External memory controller , supports ROM, SRAM, DDR2, MAP 10	Core: 1.0V, ± 10%
Interrupt controller, on-chip peripheral interrupts and 6 external interrupts	Common I/O: 3.3V, ± 10%
4-channel SpaceWire bus node controller	DDR2 and USB I/O: 2.5V, ± 10%
2-channel 1M/10M 1553B bus controller , supports BC, RT and BM	SpaceWire I/O: 2.5V, LVOS 350mV
2-channel CAN2.0 bus controller	Package
CCSDS TM I TC interfaces	784-ball Plastic (PBGA784), industrial grade
10/100M Ethernet	576 Ceramic Col (CCGA576) MIL-STD-883E/S
USB2.0 HOST controller	Environmental
Online Hardware Debug Support Unit (DSU)	Operating Temp: -40°C to +85°C - PBGA784
Timer , Watchdog, GPIO, UART, 12C, SPI	Operating Temp: -55°C to +125°C - CCGA576
Software	Storage Temp: -65°C to +150°C
IDE: Orion 6 or Eclipse	
Compiler : SPARC-GCC	
Debug Monitor: OCE DMON	
RTOS: VxWorks 6.7, eCOS, Linux 2.6, RTEMS	

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